Remarks

Applicant thanks Examiner Siddiqui for the careful examination of this application and for the clear explanation of the claim rejection and objection. In response to the Office Action of March 22, 2006, applicant amends the application as follows:

Paragraph [024] is amended to correct a typographical error.

Claim 1 is amended to incorporate all the claim limitations of claims 2 and 3.

Claims 2 and 3 are canceled from this examination.

Claims 7 and 8 are amended to properly depend from claim 1.

Claim 9 is amended to add a claim limitation to the multiplexer for interfacing the DUT with the automatic test equipment (ATE).

Claim 13 is amended to describe the invention more clearly.

Claim 16 is amended to add test module as a claim element and the claim step of multiplexing the DUT between a test module and an automatic test equipment (ATE).

Claim 18 is amended to describe the invention more clearly.

Applicant respectfully submits that as amended, the claims distinguish over the cited reference:

Claim 1

Claim 1 includes a test module that includes the multiplexer for interfacing the DUT with an automatic test equipment (ATE) operably connected to perform testing on the DUT. This element is not in any of the cited reference.

The Gearhardt test equipment "include a multiplexer circuit which allows the IC to select either a boundary scan input signal or the conventional data signal which is supplied to the IC from the normal data source. In this manner, an IC equipped for

boundary scan may be used in either a test mode or a normal operative mode."[1]

In the Lanier test equipment "[m]ultiplexer 714 is coupled to clock divider circuitry 720. Clock divider circuitry 720 is coupled to source waveform memory 734 and source sequencer 726. Multiplexer 714 is coupled to device under test 50 and clock lines 752 and 754. Multiplexer 714 is also coupled to multiplexer 716 and 718.

Multiplexer 718 is coupled to clock divider unit 724, which is in turn coupled to measure waveform memory 736. Multiplexer 716 is coupled to clock divider circuitry 722, which in turn is coupled to measure sequencer 730. Multiplexers 714, 716, and 718 each have inputs coupled to device under test 50."[2]

Neither reference discloses a multiplexer that is a part of a test module and is for interfacing the DUT with an automatic test equipment (ATE) operably connected to perform testing on the DUT.

Because the references do not disclose all the claim limitations in claim 1, applicant respectfully submits that claim 1 stands patentable over the references.

Claims 4-8

Because claims 4-8 properly depend from claim 1, applicant respectfully submits that they stand patentable at least by virtue of their dependence.

Claim 9

Claim 9 includes a test module with a multiplexer that interfaces the DUT with the automatic test equipment (ATE). Applicant respectfully submits that because Lanier does not disclose such a structure, claim 9 stands patentable over the Lanier patent.

Claims 10-15

Because claims 10-15 properly depend from claim 9, applicant respectfully submits

[1] US 5,701,309 col. 1, ll. 62-67.
[2] US 6,675,339 col. 29, ll. 3-13.

that they stand patentable at least by virtue of their dependence.

Claim 16

Claim 16 describes a method for digital testing of a semiconductor device under test (DUT) positioned in a socket on a device interface board (DIB) including a test module. The method includes a step of multiplexing the DUT between a test module and an automatic test equipment (ATE).

Applicant respectfully submits that because neither the Lanier test equipment nor the Gerahardt test equipment discloses this step, claim 16 stands patentable over the references.

Claims 17-21

Because claims 17-21 properly depend from claim 16, applicant respectfully submits that they stand patentable at least by virtue of their dependence.

Applicant respectfully submits that this application is now in allowable form and the pending claims distinguish over the cited references. Applicant respectfully requests further examination of this application and timely allowance of all pending claims.

Respectfully submitted,

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